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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,523	08/27/2003	David Hartwell	200301890-2	5458

7590 03/17/2005

HEWLETT-PACKARD COMPANY
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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,523	HARTWELL, DAVID	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 August 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to continuation application filed on 27 August 2003.

2. Claims 1 – 25 are presented for examination.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1 – 25 are rejected under the judicially created doctrine of double patenting over claims 1 - 15 of U. S. Patent No. 6,629,257 B1 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

4. Every elements of claim 1 including a phase locked loop [PLL]; a circuit; a first time, and a second timer with inputs and outputs and conditions to generate output in current application are disclosed by a claim 1 of patent.

5. The circuit having a global reset output for delivering global reset signals of claim 2 in current application is disclosed by a counter circuit of claim 1 of patent.

6. Elements of claim 3 of current application a first timer and a second timer are disclosed by claims 3, and 4 of patent.

7. Watchdog timer of claim 4 of current application is taught by claim 3 of patent.

8. Forwarded clock signals of claim 5 of current application are disclosed by claim 3 of patent.

9. External reset signal, error reset signal and a set of error reset registers in claim 6 of current application are disclosed by claim 5 of patent.

10. External reset signal generation by a voltage monitor device responsive to power transition of claim 7 in current application is disclosed by claim 6 of patent.

11. The error registers are control registers in claim 8 of current application are disclosed by claim 8 of patent.

12. The second timer and the circuit [counter] elements of claim 9 of current application are taught by claim 12 of patent.

13. The halting issuance of reset signal, and releasing of PLL of claim 10 is disclosed by claim 13 of patent.

14. Releasing of global reset after subsequent predetermined period of time and distributing the phase-aligned clock signals of claim 11 of current application is disclosed by claim 14 of patent.

15. Every steps for resetting a clocking system of claim 12 including providing input signals to a phase locked loop [PLL]; a circuit [counter]; a first time, and a second timer

and generating outputs with conditions to generate output in current application are disclosed by a claim 9 of patent.

16. Generating global reset signal of claim 13 of current application is disclosed by claim 10 of patent.

17. Generating a first timer signal as a pulsed signal and a second timer is configured to detect the presence or absence of pulsed signal of claim 14 in current application is disclosed by claim 4 of patent.

18. Generating the circuit reset signal after a delay of claim 15 in current application is disclosed by halting of issuance of reset in claim 13 of patent.

19. Forwarded clock signals of claim 16 of current application are disclosed by claim 3 of patent.

20. External reset signal, error reset signal and a set of error reset registers in claim 17 of current application are disclosed by claim 5 and 15 of patent.

21. External reset signal generation by a voltage monitor device responsive to power transition of claim 18 in current application is disclosed by claim 10 of patent.

22. The error registers are control registers in claim 19 of current application are disclosed by claim 8 of patent.

23. The second timer and the circuit [counter] elements of claim 20 of current application are taught by claim 12 of patent.

24. The halting issuance of reset signal, and releasing of PLL of claim 21 is disclosed by claim 13 of patent.

25. Releasing of global reset after subsequent predetermined period of time and distributing the phase-aligned clock signals of claim 22 of current application is disclosed by claim 14 of patent.

26. Every elements of claim 23 including a phase locked loop [PLL]; a circuit; a first time, and a second timer with means for receiving inputs and means for outputting and conditions to generate output in current application are disclosed by a claim 1 of patent.

27. Computer readable media containing instructions for execution in a processor of claim 24 in current application is inherent to computer system.

28. Electromagnetic signals carrying instructions for execution on a processor of claim 25 in current application is inherent to computer system.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application, which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am to 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Nitin C. Patel
March 16, 2005